

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

Apr 30 03 06:24p

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

P. 4
RCE
11/C W/ATT
P. Walker
6-5-03

Applicant(s): Mahajani et al.

Application No.: 10/079472

Filed: 2/19/2002

Title: Gate Dielectric Structures for

Integrated Circuits and Methods for Making
and Using Such Gate Dielectric Structures

Attorney Docket No.: MA-068

Group Art Unit: 2814

Examiner: Thao X. Le

M. Brunson
7/17/02

FAX RECEIVED

APR 30 2003

TECHNOLOGY CENTER 2800

Commissioner for Patents
Washington DC 20231

RESPONSE, PRELIMINARY AMENDMENT, AND REMARKS

Dear Sir:

Applicants request continued examination under 37 CFR § 1.114. The enclosed
Response to the Office Action of March 6, 2003, Preliminary Amendment, and Remarks
constitute the required submission.

If concerns remain, the Examiner is respectfully requested to grant an interview to discuss
the references and Response.

06/04/2003 09:58 FAX 00000004 502302 10079472

01 FC:1202 144.00 CH
02 FC:1701 500.00 DA
I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date
shown below.

07/17/2003 JARTIS 00000004 502302 10079472

01 FC:1801 750.00 DA

App No. 10/079472

1

Parveta J. Squyres

Date of Transmission

4/30/03

Received from < > at 4/30/03 8:44:35 PM [Eastern Daylight Time]

INTRODUCTORY COMMENTS

The introductory comments will respond to the rejections of the latest office action. Following, each on a new page, are all pending claims (including new claims), remarks, and a conclusion.

I. Response to Office Action

This section will respond to the rejections of the office action of March 6, 2003.

A. Status of Claims:

Claims 1, 3, 5-9, 12-15, and 20-34 are pending in the application. Claims 1, 6-7, 9, 12-15, 20-22, 24, 26, 27, and 30-31 were rejected under 35 USC 102. Claims 3, 5, 8, 23, 25, 28-29, and 32-34 were rejected under 35 USC 103.

In the final office action of March 6, 2003, the Examiner cited a new reference, Luoh et al., US Publication No. 2003/0017670. Applicants assert that all claims distinguished over Luoh et al. and all other cited references, as explained in the following remarks.

B. Claim 1 and Dependents, 102(e) Rejection: Discussion

Claim 1 was rejected under 35 USC 102(e) as being anticipated by Luoh et al. Claim 1 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process.

Referring to FIG. 2 of Luoh et al., which pictures a floating gate-memory device, the Examiner correctly asserts that the region between source and drain 19 is a channel region and that oxide layer 13 is formed by an in-situ steam generation process. Examiner also states, however, that control gate 17 is the gate conductor of a transistor.

The device pictured in FIG. 2 of Luoh et al. comprises a metal oxide semiconductor (MOS) transistor. A MOS transistor, as is well known in the art, consists of a gate conductor separated from a channel region by an oxide, the channel region located between a source and drain. The conductivity of the channel is controlled by voltage on the gate conductor.

A description of a MOS transistor is provided in Exhibit A, an excerpt from a standard text in this field, *Operation and Modeling of the MOS Transistor*, by Yannis Tsividis. In a section titled "Overview of the MOS Transistor," the text introduces the elements and basic function of such a device. Figure 1.20 in the excerpt (on page 35) shows a MOS transistor, with a channel between the source and drain. The description of this device starts on page 34:

The center part of the structure [the channel] is covered by an insulator (typically silicon dioxide, which is often referred to simply as *oxide*) ...

A low-resistivity electrode, called the *gate*, is formed on top of the oxide ...

... if the gate potential is made sufficiently positive with respect to other parts of the structure, electrons can be attracted directly below the insulator ... The number of electrons in the channel can be varied through the gate potential ...

The gate conductor, then, is separated from the channel by an insulator, and voltage on the gate conductor controls conductivity of the channel. Thus in FIG. 2 of Luoh, the gate conductor, which is separated from the channel by an insulator and controls current flow in the channel, is clearly floating gate 12, not control gate 17. The oxide layer 11 between the channel region and the gate conductor 12 was formed by thermal oxidation (see paragraph [0018] of Luoh et al.), not by an in-situ steam generation process.

In embodiments of the present invention, in contrast, the ISSG oxide is between the channel region and the gate conductor. In FIG. 1, for example, oxide layer 25 (along with other insulating layers, nitride layer 35 and oxide layer 30) is between a channel region (between

gate conductor arg. source and drain 20) and gate conductor 40. Similarly, in FIGs 2a and 2b, ISSG oxide layer 56 is between channel region 58 and gate conductor 54.

Thus Luoh et al. fails to teach each and every limitation of claim 1 and its dependent claims 3, 5-8, and 28-29.

C. SONOS Claims, 102(e) Rejection: Discussion

Claim 9, 12-15, 20-22, 24, 26-27, and 30-31 were rejected under 35 USC 102(e) as anticipated by Luoh. All of these claims directly or indirectly include the limitation that the device is a "SONOS device" (eg. Claim 9), a "SONOS semiconductor device" (eg. claim 24) or a "SONOS transistor" (eg. claim 27.)

Semiconductor nonvolatile memory devices that operate by storing charge fall largely into two categories: floating gate and SONOS.

SONOS is a well-known term of art. In a SONOS device, which typically operates as a memory cell, an oxide-nitride-oxide (ONO) dielectric structure separates a gate conductor, usually of silicon, from a channel, also usually of silicon. The sequence of contiguous layers, silicon-oxide-nitride-oxide-silicon, gives the SONOS device its name. The term MONOS is also used to describe a variation on these devices, in which metal replaces silicon in the gate conductor. An example of a SONOS device appears in FIG. 1 of the present application. Oxide layer 25, formed by ISSG, is a tunnel oxide. Charge is stored in nitride layer 35.

In contrast, in a floating gate device, as in FIG. 2 of Luoh et al., charge is stored not in a nitride layer, but in an electrically isolated or "floating" gate, normally of silicon. The device pictured in FIG. 1 of Luoh et al. is a floating gate device, containing floating gate 12.

An excerpt from Volume 28 of *Cx-News*, a semiconductor technical information online publication from Sony Electronics, is included in Exhibit B. In the second paragraph, this article gives an example of the terms "SONOS", "MONOS" and "floating gate" as used in the art:

Figure 1 compares the MONOS and floating gate device structures. As can be seen in Figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data.

The MONOS device shown in Figure 1 of the Sony publication and the SONOS device of Fig. 1 of the present application both show a silicon channel, and, on the channel and in contiguous contact, an oxide layer, a nitride layer, a second oxide layer, and a gate conductor. In the SONY publication the gate conductor is metal, and in the present application it may be silicon. The Sony publication notes both the metal (MONOS) and silicon (SONOS) gate conductor variations. Similarly, the present application notes that the SONOS gate conductor is "typically of polysilicon, metal, or a silicide" (paragraph [19].)

It will be seen that the floating gate device pictured in Figure 1 of the Sony publication is essentially the same as the floating gate device in Fig. 2 of Luoh et al. In both, there is a channel, then on the channel and in contiguous contact, an oxide, a polysilicon floating gate, a dielectric layer, and a control gate. The difference lies in the dielectric between the floating gate and the control gate: In the Sony publication, this dielectric layer is a single layer of silicon dioxide, while in Fig. 2 of Luoh, the dielectric comprises layers 13-16, which are oxide, nitride, oxynitride, and oxide layers respectively, all dielectrics. As noted in paragraph [0004] of the Description of Prior Art in Luoh et al.:

In conventional stacked non-volatile semiconductor memory devices, an insulating layer for insulating a floating gate and a control gate from each other is a single layer of silicon dioxide ...

In Luoh et al., the oxide-nitride-oxynitride-oxide stack is developed to provide better insulation between the floating gate 12 and the control gate 17, as the Description of Prior Art makes clear.

The Examiner asserts of the floating gate device pictured in FIG. 2 of Luoh et al. that:

... the device is a SONOS transistor 10=silicon, 13=oxide, 14=nitride, 16=oxide,
17=silicon ...

The fact that the Examiner is able to identify non-contiguous layers distributed throughout a floating gate device that coincidentally correspond to the contiguous layers of a SONOS device does not make the device a SONOS device. In fact, Luoh names and teaches against even using an ONO structure (paragraphs [0005] and [0006]), the heart of a SONOS device, as insulation between the control gate 17 and the floating gate 12, arguing that the structure becomes prone to pinholes and other problems as device densities increase.

Additionally, claim 9 teaches a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer. An embodiment of this structure is illustrated in FIG. 1 of the present application.

ON argument
(Several factors, including the dictionary meaning of the word "on" ("Used to indicate position above and supported by or in contact with," is the first definition found in the American Heritage Dictionary), the drawing of FIG. 1, and the well-known structure of a SONOS device,

give clear indication that the layers recited in this claim are contiguous, not distributed as in the reference.

Thus Luoh et al. fails to teach each and every limitation of claims Claim 9, 12-15, 20-22, 24, 26-27, and 30-31.

D. 35 USC 103 Rejections: Discussion

Claims 3, 5, 8, 23, 25, 28-29, and 32-34 were rejected under 35 USC 103 as being unpatentable over Luoh et al.

The Examiner's 103 rejection of claim 3 is the following:

Pre-empt

Regarding to claim 3, Luoh does not expressly disclose the transistor is a thin film transistor (TFT).

However, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG dielectric structure of Luoh for intended use.

No further elaboration is offered. MPEP 2143 describes the basic requirements of a *prima facie* case of obviousness:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

As no attempt is made by the Examiner to identify a suggestion to modify the reference, Applicants submit that a *prima facie* case of obviousness has not been established. The same applies to the 103 rejection for claims 5, 8, 23, 25, and 28, which have the same rationale.

The Examiner's discussion of the 103 rejection of claims 29, 32, and 33 is the following:

Regarding to claim 29, 32-33, Luoh discloses a transistor comprising a floating gate 12, fig. 2.

With no summary or conclusion, Applicants cannot determine what the Examiner intends to assert, and thus are unable to address it.

Regarding claim 34, this claim depends from claim 27, which teaches that the device is a SONOS device. As described in the previous section, the reference thus cannot teach each and every limitation of claim 34.

Claims 1, 3, 5, 8, 23, 25, 28-29, and 32-34 are rejected under 35 USC 103 as being unpatentable over US Patent No. 5932484 to Iwanaga et al. in view of Luoh et al.

Regarding claim 1, 23, and 25, the Examiner notes that Iwanaga et al. does not expressly disclose an oxide layer formed in an in-situ steam generation process. The Examiner asserts that the substitution of the oxide layer of Iwanaga et al. with the ISSG oxide layer of Luoh et al. would have been obvious:

... because it would have created dielectric structure having higher withstanding voltage, lower current leakage, improved retention characteristic of memory cell, single-wafer process, and reduce the structure stress as taught by Luoh [0009] and [0010].

The cited paragraphs of Luoh et al. read as follows:

[0009] It is another objective of the present invention to provide a method for forming a gate dielectric stack of silicon dioxide/silicon nitride/silicon oxynitride/silicon dioxide by a single-wafer thermal process.

[0010] It is a further objective of the present invention to provide a method for manufacturing a semiconductor memory device with a gate dielectric stack, which can reduce the structural stress.

Applicants find no suggestion here to replace the oxide of a dielectric structure interposed between a gate electrode 4 and a channel of a TFT device (as in Fig. 1a of Iwanaga et al.) with the oxide of an oxide-nitride-oxynitride-oxide dielectric structure interposed between a floating gate 12 and a control gate 17 in a floating gate memory device (as in Fig. 2 of Luoh et al.) As

these oxide layers exist at different levels in distinct stacks in unrelated devices, Applicants believe such a substitution is in no way obvious.

The 103 rejection of claims 5 and 8 rely on the same cited paragraphs, [0009] and [0010], to suggest that it would have been obvious to replace the oxide of Iwanaga et al. with an ISSG oxide created at a temperature ranging from 600 to about 900 degrees C, and annealing the oxide layer in a nitric oxide atmosphere. As before, Applicants find no such suggestion in these paragraphs.

Regarding the rejection of claims 28, 29, and 32-33, the Examiner asserts:

Regarding to claims 28, 29, 32-33, Iwanaga, disclose the method wherein the transistor is a SONOS transistor, having a floating gate.

Applicants cannot accept this characterization of the device disclosed in Iwanaga et al. As described earlier, a device is either a SONOS device or a floating gate device, and thus cannot be "a SONOS transistor, having a floating gate." While Iwanaga et al. do not use the term SONOS, the reference does teach a gate conductor separated from a channel by a silicon oxide-silicon nitride-silicon oxide sandwich, apparently the elements of a SONOS stack. But Applicants find nothing in Iwanaga et al. that could in any way be construed as a floating gate. Thus Iwanaga et al. and Luoh et al. cannot teach each and every limitation of those claims.

PTO/SB/17 (01-03)

Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**FEE TRANSMITTAL
for FY 2003**

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 1170.00)

Complete if Known

Application Number	10/079472
Filing Date	February 19, 2002
First Named Inventor	Maitreyee Mahajani et al
Examiner Name	Thao X. Lu
Art Unit	2814
Attorney Docket No.	MA-068

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☒ Deposit Account:

Deposit Account Number	502302
Deposit Account Name	Matrix Semiconductor, Inc.

The Commissioner is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.
FEE CALCULATION**1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 750	2001 375	Utility filing fee	
1002 330	2002 165	Design filing fee	
1003 520	2003 260	Plant filing fee	
1004 750	2004 375	Reissue filing fee	
1005 180	2005 80	Provisional filing fee	

SUBTOTAL (1) (\$ 00)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
8	-20** = 0	18.00	0.00
8	-3** = 5	84.00	420.00
		0.00	0.00

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1202 18	2202 9	Claims in excess of 20	
1201 84	2201 42	Independent claims in excess of 3	
1203 280	2203 140	Multiple dependent claim, if not paid	
1204 84	2204 42	** Reissue independent claims over original patent	
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) (\$ 420.00)

*or number previously paid, if greater. For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	1053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for ex parte examination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 410	2252 205	Extension for reply within second month	
1253 930	2253 465	Extension for reply within third month	
1254 1,450	2254 725	Extension for reply within fourth month	
1255 1,970	2255 985	Extension for reply within fifth month	
1401 320	2401 160	Notice of Appeal	
1402 320	2402 160	Filing a brief in support of an appeal	
1403 280	2403 140	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,300	2453 650	Petition to revive - unintentional	
1501 1,300	2501 650	Utility issue fee (or reissue)	
1502 470	2502 235	Design issue fee	
1503 630	2503 315	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	1806 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (limits number of properties)	
1809 750	2809 375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 750	2810 375	For each additional invention to be examined (37 CFR 1.129(b))	
1801 750	2801 375	Request for Continued Examination (RCE)	750.00
1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 750.00)

SUBMITTED BY

Name (Print/Type) Pamela J. Squyres

Registration No.

52,246

(Complete if applicable)

Telephone (408) 856-2921

Signature

Date April 30, 2003

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Signature

Date April 30, 2003

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

Received from < > at 4/30/03 8:09:17 PM [Eastern Daylight Time] completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

10/079472

Matrix Memory

Matrix Semiconductor, Inc.
3230 Scott Boulevard Santa Clara, California 95054
Telephone 408.969.4848 Facsimile 408.969.4849

FAX RECEIVED

April 30, 2003

APR 30 2003

TECHNOLOGY CENTER 2800

Time: _____
(Santa Clara, California)

TO: Commissioner for Patents
Attn: Thao X. Le
Patent Examining Corps
Facsimile Center
Washington, D.C. 20231

FROM: Pamela J. Squyres

OUR REF: MA-068

TELEPHONE: 408-869-2921

FAX NUMBER 703-308-7722

* Please deliver to Examiner Thao X. Le in Art Unit 2814. *

Document(s) Transmitted: Fax Cover Sheet (1 pg)
Fee Transmittal in duplicate (2 pgs)
Response, Preliminary Amendment and Remarks
with Exhibits A&B (29 pgs)
Interview Summary (1 pg)

Total pages of this transmission, including cover letter: 33 pgs.

If you do NOT receive all of the pages described above, please telephone us at 408-869-2921, or fax us at 408-869-8923.

In re. Patent Application of: Maitreyee Mahajani et al.

Examiner: Thao X. Le

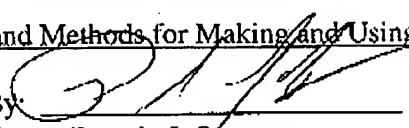
Serial No.: 10/079472

Group Art Unit: 2814

Filed: February 19, 2002

Docket No.: MA-068

Title: Gate Dielectric Structures for Integrated Circuits and Methods for Making and Using Such Gate Dielectric Structures

By: 
Name: Pamela J. Squyres
Reg. No.: 52,246

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.


Pamela J. Squyres

4/30/03
Date of Transmission